ABSTRACT

A pipelined analog-to-digital converter features an amplifier block that includes a switching network to implement a double sampling and double conversion principle of operation. The amplifier block utilizes both phases of a clock for sampling and conversion. Additionally, each stage of the analog-to-digital converter is associated with two independent processing blocks. The analog-to-digital converter can achieve double throughput for approximately the same level of power consumption. Alternatively, throughput may be maintained, but the gain-bandwidth of the amplifier block may be reduced by half, thereby halving the DC bias current consumed by the amplifier. Additionally, the output signal of the amplifier itself is not reset to a common mode voltage.